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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,670	EKNER ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-27 and 29-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 15-27, 29-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/03/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 02/03/2006.

2. Claims 1-13, 15-27 and 29-41 are pending in this application. Claims 2, 15, and 29 are independent claims. In Amendment, claims 14, 28 and 42 are cancelled. This Office Action is made non-final after a RCE filed 02/03/2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 9-13, 15, 23-27, 29, and 37-41 are rejected under 35 U.S.C. 103(a) as being obvious over Weng et al. (U.S. 6,199,088) in view of Miyazaki (U.S. 5,181,183).

Re claim 1, Weng et al. disclose in Figures 2-3 a multiply unit (abstract and all component in Figure 2) comprising: at least one input data path (e.g. paths for receiving A and B into 12 as example) for receiving one or more input operands (e.g. A and B) to the multiply unit (e.g. all components in Figure 2); an arithmetic multiplier (e.g. multiplier for multiplying $B*A^{-1}$) connected to receive the one or more input operands (e.g. B); a binary polynomial multiplier (e.g. 12, 14, and half multiplier) connected to receive the one or more input operands (e.g. A and output of permutation circuit) and

including components separate and distinct from components of the arithmetic multiplier (e.g. polynomial multiplier is 12, 14, and half multiplier wherein the arithmetic multiplier is the multiplier of $B*A^{-1}$), and permutation logic (e.g. permutation circuit of A^{2M} as seen in Figure 2) connected to receive the one or more input operands (e.g. A) and operable to produce an output (e.g. output of 105 in Figure 3) comprising a permutation of the one or more input operands (e.g. $A^{2\wedge M}$) and a multiply unit output data path (e.g. output of Figure 2 or 3) connected to receive an output of the arithmetic multiplier (e.g. 108) and connected to receive an output of the binary polynomial multiplier (e.g. 106) and connected to receive the output of the permutation logic (e.g. 105). Weng et al. do not disclose the multiply unit output data path includes one or more components to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result. However, Miyazaki discloses in Figure 1 the multiply unit output data path includes one or more components (e.g. part 309 in Figure 1) to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic (e.g. either output result of 303 or 305 which corresponding to combining circuit or permutation circuit in Figure 1) to form a result (e.g. col. 2 lines 5-25). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a component in a multiply unit to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result as seen in Miyazaki's invention into Weng et al.'s

invention because it would enable to efficiently and flexibility outputting selected result for used in sub-sequence (e.g. col. 2 lines 8-12).

Re claim 9, Weng et al. further disclose in Figures 2-3 the binary polynomial multiplier includes a binary polynomial multiplication array (e.g. col. 6 line 20 and lines 40-57).

Re claim 10, Weng et al. further disclose in Figures 2-3 the binary polynomial multiplier includes a polynomial multiplication array having a first input and a second input (e.g. A and output of permutation circuit), the polynomial multiplication array including: a plurality of row multipliers (e.g. half multiplier) that multiply the first input by a bit of the second input; and at least one adder (e.g. col. 6 line 20) for computing a result by adding the results from the plurality of row multipliers.

Re claim 11, Weng et al. further disclose in Figures 2-3 the at least one adder performs a bit-wise exclusive-or on the results from the plurality of row multipliers (e.g. col. 5 lines 37-40).

Re claim 12, Weng et al. further disclose in Figures 2-3 at least one of the pluralities of row multipliers performs multiplication by computing a logical AND of the first input and a bit of the second input (e.g. col. 5 lines 65-67 and col. 6 lines 1-11).

Re claim 13, Weng et al. further disclose in Figures 2-3 further comprising an accumulator, and wherein the at least one adder computes a result by adding the results from the plurality of row multipliers and the accumulator (e.g. col. 5 line 66 and col. 6 line 20).

Re claim 15, it is a processor claim of claim 1. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 23, it is a processor claim of claim 9. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 24, it is a processor claim of claim 10. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 25, it is a processor claim of claim 11. Thus, claim 25 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 26, it is a processor claim of claim 12. Thus, claim 26 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claim 27, it is a processor claim of claim 13. Thus, claim 27 is also rejected under the same rationale in the rejection of rejected claim 13.

Re claim 29, it is a computer-readable medium claim of claim 1. Thus, claim 29 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 37, it is a computer-readable medium claim of claim 9. Thus, claim 37 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 38, it is a computer-readable medium claim of claim 10. Thus, claim 38 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 39, it is a computer-readable medium claim of claim 11. Thus, claim 39 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 40, it is a computer-readable medium claim of claim 12. Thus, claim 40 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claim 41, it is a computer-readable medium claim of claim 13. Thus, claim 41 is also rejected under the same rationale in the rejection of rejected claim.

5. Claims 2-6, 16-20, and 30-34 are rejected under 35 U.S.C. 103(a) as being obvious over Weng et al. (U.S. 6,199,088) in view of Miyazaki (U.S. 5,181,183), as applied to claims 1, 15, and 29 above, and further in view of Bhandal et al. (U.S. 6,711,602).

Re claims 2-6, Weng et al. in view of Miyazaki do not disclose in Figures 2-3 the arithmetic multiplier includes a Wallace tree multiplier array including a plurality of carry-save adders arranged in a tree structure and a carry-propagate adder wherein the multiplier utilizing Booth recoding logic. However, Bhandal et al disclose in Figures 5-8 the arithmetic multiplier includes a Wallace tree multiplier array (e.g. all levels of CSA in Figure 7) including a plurality of carry-save adders (e.g. CSA) arranged in a tree structure (e.g. all levels of CSA arrangement) and a carry-propagate adder wherein the multiplier utilizing Booth recoding logic (e.g. 710b). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the arithmetic multiplier includes a Wallace tree multiplier array including a plurality of carry-save adders arranged in a tree structure and a carry-propagate adder wherein the multiplier utilizing Booth recoding logic as seen in Bhandal et al.'s invention into Weng et al. in view of Miyazaki's invention because it would enable to reduce the circuitry complexity and increase the system performance.

Re claim 16 it is a processor claim of claim 2. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 17, it is a processor claim of claim 3. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 18, it is a processor claim of claim 4. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 19, it is a processor claim of claim 5. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 20, it is a processor claim of claim 6. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 30, it is a computer-readable medium claim of claim 2. Thus, claim 30 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 31, it is a computer-readable medium claim of claim 3. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 32, it is a computer-readable medium claim of claim 4. Thus, claim 32 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 33, it is a computer-readable medium claim of claim 5. Thus, claim 33 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 34, it is a computer-readable medium claim of claim 6. Thus, claim 34 is also rejected under the same rationale in the rejection of rejected claim 6.

6. Claims 7-8, 21-22, and 35-36 are rejected under 35 U.S.C. 103(a) as being obvious over Weng et al. (U.S. 6,199,088) in view of Miyazaki (U.S. 5,181,183) in further view of Bhandal et

al. (U.S. 6,711,602), as applied to claims 2, 16, and 30 above, and further in view of Magar (U.S. 4,538,239).

Re claims 7, Weng et al. do not in view of Miyazaki in further view of Bhandal et al. disclose in Figures 2-3 the arithmetic multiplier performs 32-bit by 16 bit multiplications in a two clock cycles. However, Magar disclose in Figure 3 that an arithmetic multiplier performs 16x16 multiplications in a two clock cycles back in 1985. As the technology improve, more multiplications can be processed in less cycles. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to perform 32x16 multiplications in a two clock t cycles as seen in Magar's invention into Weng et al. in view of Miyazaki in further view of Bhandal et al. 's invention because it would enable to increase the system performance.

Re claim 8, Weng et al. in view of Miyazaki in further view of Bhandal et al. do not disclose in Figures 2-3 the arithmetic multiplier performs 32-bit by 32 bit multiplications in three clock cycles. However, Magar disclose in Figure 3 that an arithmetic multiplier performs 16x16 multiplications in a two clock cycles back in 1985. As the technology improve, more multiplications can be processed in less cycles. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to perform 32x32 multiplications in a three clock cycles as seen in Magar's invention into Weng et al. in view of Miyazaki in further view of Bhandal et al.' s invention because it would enable to increase the system performance.

Re claim 21, it is a processor claim of claim 7. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 22, it is a processor claim of claim 8. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 35, it is a computer-readable medium claim of claim 7. Thus, claim 35 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 36, it is a computer-readable medium claim of claim 8. Thus, claim 36 is also rejected under the same rationale in the rejection of rejected claim 8.

Response to Arguments

7. Applicant's arguments filed 02/03/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 10-11 for claims rejected under Weng et al. and Miyazaki et al. that Miyazaki et al. do not teach or suggest either a binary polynomial multiplier or an arithmetic multiplier as disclosed in the claim. Further, Miyazaki et al. do not disclose the missing element of the multiply unit output data path includes one or more components to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result as clearly cited in the claims.

The examiner respectfully submits that cited secondary reference by Miyazaki clearly discloses a circuit capable of performing an arithmetic (e.g. by 330 in 310 unit), addition, subtraction (e.g. 301), and permutation (e.g. 307) in Figure 1. The missing element or feature in the primary reference is the selector, multiplexer, or switch means for selecting either the output results of polynomial multiplier, an multiplier, and

permutation. Clearly, the secondary reference discloses the missing element or feature above as the switch (e.g. 309 in Figure 1 or 409 in Figure 2) for switching, selecting, or multiplexing either the output results of permutation circuit 304 (e.g. wherein 305 as a register for storing the result of permutation circuit 304) and addition/subtraction circuit 301 (e.g. wherein 303 as a register for storing the result of the combining circuit). Mainly, the secondary reference by Miyazaki et al. discloses a missing feature or element in the primary reference as a switch for selecting multiple inputs as clearly seen in Figure 1 element 309.

b. The applicant argues in pages 12-13 generally for claims rejected under Weng et al. and Miyazaki et al. that there is no motivation to combine the references to achieve the applicant's invention and Miyazaki is an non-analogous art which the Office action impermissibly relies on hindsight reconstruction.

The examiner respectfully submits that the motivation to combine the missing element or feature in the primary reference is clearly cited in the Office action as it would enable to efficiently and flexibility outputting selected result for used in sub-sequence (e.g. col. 2 lines 8-12). The functionality and capability of a switch, a selector, or a multiplexer is well-known by any person having ordinary skill in the art at the time the invention is made which is used to efficiently and flexibility outputting a selection from multiple inputs. Further, the secondary reference by Miyazaki is also an analogous art with the pending application, which is a

hardware solution for processing digital information comprising basis hardware components as multiplier, adder, subtractor, selector...

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
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June 14, 2006

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